Custom No.: 31561
Application No.: 10/707,082
Docket No.: 11690-US-PA

To the Drawings

Applicant found the Fig.1 and Fig.2 are not annotated with a legend of "Prior Art." So, these two drawings are accordingly amended.

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REMARKS

Present Status of the Application

Claims 1-14 remain pending of which claims 1, 5, 7 and 12-13 have been amended without prejudice or disclaimer in order to more explicitly describe the claimed invention. It is believed that no new matter adds by way of amendments made to claims. to more clearly describe the claimed invention. Moreover, Figs. 1 and 2 are so amended to be annotated with a legend of "Prior Art." For at least the following reasons, Applicant respectfully submits that claims 1-14 are in proper condition for allowance. Reconsideration is respectfully requested.

Discussion of amendments made to the claims

From the paragraph [0028] in the specification, there discloses" a circuit block 502, for example, is disposed between an original selection signal CSL0 and the column selection line 306..., and the final row selection signal EQSEL is coupled to the row selection line 308," Accordingly the claims 1 and 7 are amended to incorporate a limitation of "a column selection line coupled to a first circuit block and a row selection line coupled to a second circuit block.

Moreover, in paragraph [0032] in the specification and Fig.8, there discloses" the FSCSL and FSEQSEL of a defective memory block are in a high state, no matter whether it is in an active or stand-by state. Therefore, the CSL of the column selection line 306 and the EQSEL of the row selection line 308 have the same state as the STBY," Accordingly the claims 1 and 7 are amended to add a limitation of "the first circuit block is capable of outputting a row turn-off signal when a defect memory cell is detected, and the second

circuit block is capable of outputting a row turn-off signal when the defect memory cell is detected." Eventually, in paragraph [0038], there discloses "the leakage current generated from the defective memory cells and power consumption are reduced by, for example, turning off all defective memory cells." Accordingly the claims 1 and 7 are amended to add a limitation of "breaking a leakage current path existing in the defect memory cell."

Discussion of the claim objections

3. Claim 13 is indicated to be dependent from claim 7, and further comprising a second circuit block...There is no "first "circuit block disclosed in claim 7 except in claim 12 so that claim 13 should be dependent from claim 12.

In response thereto, as the claim 7 is so amended to incorporate "a second circuit block," the claim 13 is able to dependent from the claim 7.

Discussion of " Response to Arguments" as stated in this OFFICE ACTION

4. Contrary to the remarks, page 8, last paragraph in the latest response, it appear that this disclosure of the application does not disclose any device or method repairing defective memory cell.

In response thereto, from the paragraph [0007] (i.e. "SUMMARY OF INVENTION"), the present application intends to solve the problems of power consumption and rise of temperature resulting from the leakage current, rather than repairing defective memory cell as stated in the latest response. Accordingly, to more clarifying an objective of the present application, the claims 1, 5 and 7 are so amended to

include the feature of "breaking a leakage current path existing in the defect memory cell by disconnecting its connection to a power supply terminal."

6. Claims 1, 2, 5 and 7are rejected under 35 U.S.C. 102(e) as being anticipated by Sakimura et al. (US-6,885,579, hereinafter Sakimura).

In response thereto, applicant traverses the preceding rejection based on the following argument. To establish a prima facie case of anticipation, the prior reference (i.e. Sakimura) should teach, suggest or disclose all limitations of independent claims 1, 5 and 7. From the prior art of Sakimura, it intends to eliminate parasitic electric current that damages reliability of data stored in a memory cell, instead of breaking a leakage current path existing in the defect memory cell as claimed in the amended claims 1, 5 and 7. Actually, parasitic electric current as disclosed in Sakimura, is totally distinct from the claimed leakage current path because the parasitic electric current is intrinsic electric current and must occurs in any to-be-read memory cell; rather, the leakage current path happens to any defect memory cell in which its gate is shorted to its source/drain as a result of there existing some random defects in manufacturing the

memory.

Secondly, in re amended claims 1 and 7, the examiner alleged that a column selection line and a row selection line are identical to bit lines 4 and word lines 3 as disclosed in Fig.4, in Sakimura, respectively. However, the examiner's preceding allegations are incorrect because, in Sakimura, the bit lines 4 and word lines 3 are used to read data stored in a selected memory cell; instead, in claims 1 and 7 of the present application, the column selection line and the row selection line are coupled to a first circuit block and a second circuit block, respectively, so as to be capable of receiving a column turn-off signal and a row turn-off signal, respectively, when a defect memory cell is detected. Thus, the column selection line and the row selection line as claimed in the amended claims 1 and 7 are not identical to bit lines 4 and word lines 3 as disclosed in Fig.4, in Sakimura. Thirdly, the examiner alleged that a switch device as claimed in the amended claims 1 and 7 is identical to switch device X-selector 11 and Y-selector 13 as disclosed in Fig.4, in Sakimura. However, as the examiner incorrectly presumed bit lines 4 and word lines 3 as disclosed in Fig.4, in Sakimura, are identical to the column selection line and the row selection line, respectively, actually, the switch device as claimed in the amended claims 1 and 7 is not identical to switch device X-selector 11 and Y-selector 13 as disclosed in Fig.4, in Sakimura.

In short, Sakimura fails to teach, suggest or disclose every element including the column selection line, the row selection line and the switch device, as claimed in the amended claims 1 and 7. In other words, the amended claims 1 and 7 are not anticipated by Sakimura and thus patentable.

Regarding the amended claim 5, as discussed above, since Sakimura fails to disclose the same device as those claimed in the amended claims 1 and 7, it accordingly is impossible to permit Sakimura to disclose the same operating method as the amended claim 5 with a totally different device. In other words, the amended claim 5 is not anticipated by Sakimura and thus patentable.

Regarding the dependent claim 2, it should be patentable as a matter of law for the reason that it contains all limitations of its allowable base claim 1.

Discussion of the claim rejection under 35 USC 103

8. The Office Action rejected claims 4, 6, 10 and 11 under 35 U.S.C. 103(a) as being unpatentable over Sakimura in view Arimoto et al. (US-2003/0103368, hereinafter Arimoto).

In response thereto, applicant traverses the preceding rejection based on the following argument. To establish a prima facie case of obviousness, the cited references (i.e. Sakimura and Arimoto) not only should provide the desirability (or motivation) to modify the references, but should disclose all limitations of the claims 4, 6, 10 and 11. Fist of all, Sakimura and Arimoto fail to provide the desirability because of their different intended-to-solve problems. As the claims 4, 6, 10 and 11 are dependent claims, they contain all limitations of their corresponding allowable base claims 1, 5 and 7, which are not disclosed by Sakimura, as discussed above. Thus, even if Sakimura and Arimoto could be combined, this combination still fails to render the claims 4, 6, 10 and 11 obvious because neither Sakimura nor Arimoto discloses their all limitations. In other words, the claims 4, 6, 10 and 11 are patentable.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-14 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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